EF1SRP-05U Supplement (4571Group Edition)

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Suisei Electronics System Co., Ltd.

1. General Description

This supplement contains information on matters that require attention for reading and writing data to Renesas Technology Corp. 4571 Group MCU with built-in QzROM.

2. Operating Environment

Please use the MCU mentioned in this supplement in the environment as follows.

＜EFP-I＞
Monitor Version ：Ver.4.18.15 or later
＜EFP-1M＞
Monitor Version ：Ver.4.A8.15 or later
＜WinEfpRE Control Software＞
WinEfpRE Version ：Ver.1.30.05 or later

＜EFP-S2 or EFP-S2V＞
Monitor Version ：Ver.1.00.54 or later
＜EFP-S2 or S2V Control Software＞
WinEFP2 Version ：Ver.1.02.23b or later

3.Pin Connection

Table 3.1 lists the connection of target connection cable pin of the 4571 Group.

Table 3.1: List of Target Connection Pin

Connection Pin No. (EF1SRP-05U side)	Target End Wire Color	Signal	3-Wire Cable Pin No.	MCU Connection Pin in Serial I/O Mode	I/O (Writer side)
1	Orange/red dotted 1	GND	NC	Connects to VSS pin *2	—
2	Orange/black dotted 1				
3	Gray/red dotted 1	T_VPP	2	Connects to K pin	Output
4	Gray/black dotted 1	T_VDD	3	Connects to VDD pin *1	I/O
8	White/black dotted 1	T_PGM/OE/ MD	6	Connects to P10 pin	Output
9	Yellow/red dotted 1	T_SCLK	4	P00	Output
10	Yellow/black dotted 1	T_TXD	5	Connects to P01 pin *3	Output
11	Pink/red dotted 1	T_RXD			Input
12	Pink/black dotted 1	T_BUSY	1	Unconnected	NC
14	Orange/black dotted 2	T_RESET	7	Connects to RESET pin *4	Output
15	Gray/red dotted 2	GND	8	Connects to VSS pin *2	—
16	Gray/black dotted 2				

Supplement of Pin Treatment:

*1 Power Supply Connection

In case user consumption current is high (20mA or more except MCU), please provide VDD power from user target side. VDD power should not be supplied from EFP-I.

Moreover VDD power supply range during serial EPROM mode is to be 2.7V to 4.7V.

*2 GND Connection

The signal GND has 4 pins (No.1, 2, 15 and 16) of EF1SRP-05U side connector. When connecting to the target board, you can connect with using only 1 pin, but connecting 2 or more pins is recommended.

*3 SDA Connection

Please pull up with 1kΩ resistance during serial I/O mode.

*4 RESET Connection

RESET cancel in MCU is not carried out during using a writer. To execute user program, you should therefore unplug the user target connection to the writer. As for RESET output at writer side, see Note 2 in the page 3.

(1) Fig3.1 shows an example of target MCU peripheral circuit when using 4571 group.

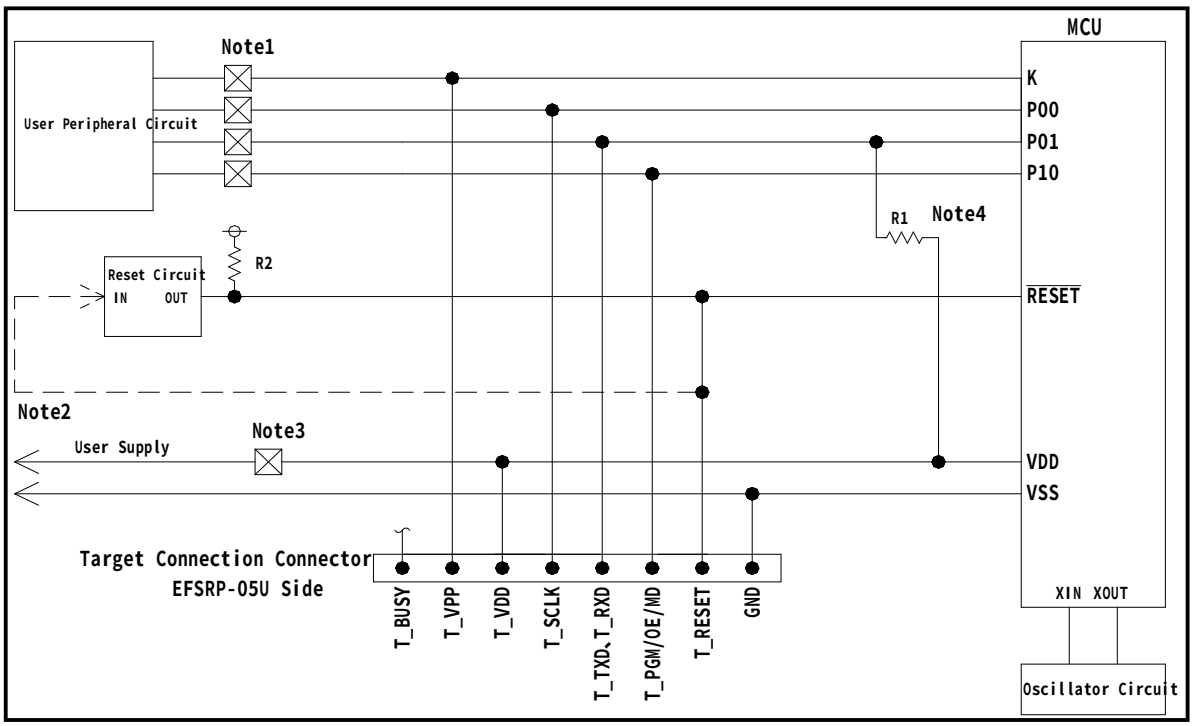


Fig3.1: Target MCU Peripheral Circuit Example

*Notes:

1: If the user peripheral circuit is an output circuit, you should disconnect by jumper to avoid output collision when executing serial I/O mode.

2: EFP-I side RESET output is an open collector, therefore connect to the RESET pin with 1kΩ pull-up processing if RESET circuit is open collector output. If the RESET circuit is CMOS output, disconnect by jumper as described in Notes 1, or connect the EFP-I side T_RESET signal to RESET circuit input.

3: In case user consumption current is high (20mA or more except MCU), user power supply should be separated. Please connect so that EFP-I side T_VDD is to be supplied to MCU.

4. In a serial input and output mode, please make pull-down by resistance of 1kΩ.

4.Relation Between VDD Voltage and Clock Timing

Transfer rate of clock synchronization type communication for T_SCLK signal needs to be changed according to the level of VDD voltage supplied to target MCU. In case VDD power is supplied from writer, baud rate should be set automatically. On the other hand, the baud rate should be set manually in case VDD power is supplied from user target.

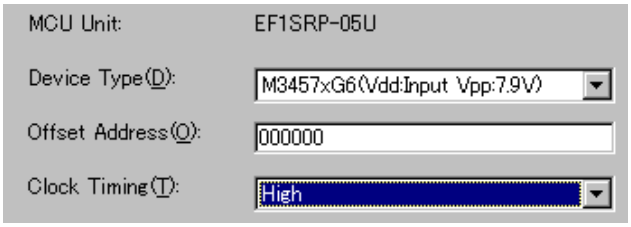
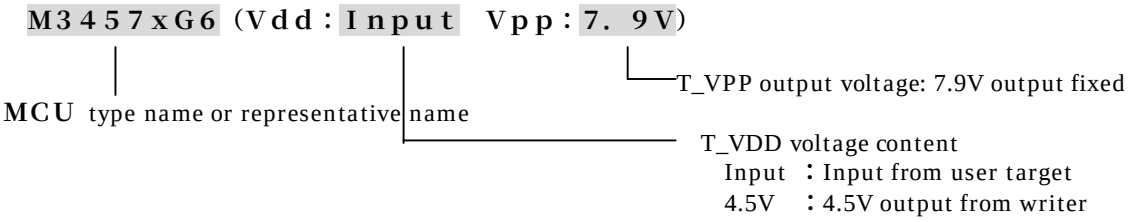


Fig.4.1: Clock Timing Setting Screen

< How to Switch T_VDD Power Supply >

VDD I/O can be switched with the setting of Device Type in Environment Setting dialog.



< Switch Condition and Setting Method of T_SCLK Baud Rate >

Please switch the setting of Clock Timing in Environment Setting dialog, according to voltage value of T_VDD supplied as MCU operation power.

2.7V to 4.7V: Clock transfer rate should be 500kbps or below. Clock Timing setting should be Low.

4.0V to 4.7V: Clock transfer rate should be 1Mbps or below. Clock Timing setting should be High.

5. Read Protect Function

4571 group MCU is equipped with a read protect function to prevent unauthorized data read, and thereby the protect function can be set on writer side. The below shows how to set the read protect function.

<How to Set Read Protect>

The command can be executed after a box of "Writing of a Protection bit (W)" in the execution dialog of Program, Verify and Device Micro Command is checked.

Only when each command is terminated normally, the read function is set to take effect. (Refer to F ig5.1).

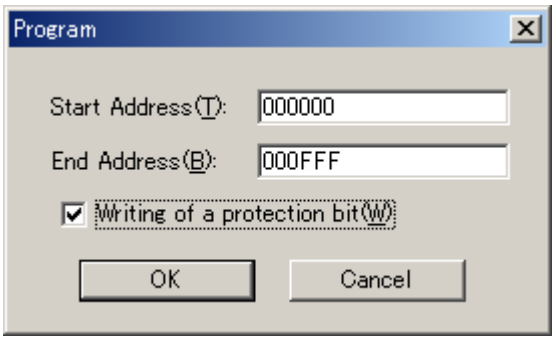


Fig5.1: Read Protect Function Setting Screen

<MCU after setting Read Protect>

When you carry out Read and Program, Read protection error occurs and command stops it for MCU that Read protection function became effective.

* There is no method to invalidate Read protection function. Please be careful about the setting of Read protection function enough.

6.Writing Adapter

In order for MCU single writing, writing adapter for serial I/O mode is on sale.

Fig6.1 lists products of writing adapter.

Fig.6.1 : Writing Adapters for 4571 group Serial I/O mode

Product Type	Corresponding Package	Corresponding MCU
MS4502-24F	24P2Q-A	M34571G4FP, M34571G6FP, M34571GDFP,

* For price, etc. of each writing adapter, please contact our distributor or us.